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10EC56

Fifth Semester B.E. Degree Examination, May 2017
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain with neat sketches of NMOS fabrication. **(10 Marks)**
b. Derive the expression for V_{out} at region C of CMOS inverter characteristic plot **(05 Marks)**
c. What is latch up phenomenon? **(05 Marks)**

2 a. Draw the schematic, stick and layout of CMOS NAND gate. **(08 Marks)**
b. Explain the design rules with neat diagrams for diffusion, metal and transistor. **(07 Marks)**
c. What are the different types of contacts? Explain. **(05 Marks)**

3 a. Explain pseudo NMOS logic, dynamic CMOS and clocked CMOS logic. **(15 Marks)**
b. Explain 2 input XNOR gate in pass transistor logic. **(05 Marks)**

4 a. Derive the expression for delay (τ) in terms of sheet resistance and area capacitance for NMOS inverter and CMOS inverter circuit. **(10 Marks)**
b. Find the scaling factors for following MOS circuits : (i) Gate capacitance (ii) Gate delay (iii) Saturation current (iv) Current density (v) Power dissipation. **(10 Marks)**

PART – B

5 a. Explain the structured design of a parity generator with necessary blocks and stick diagrams. **(10 Marks)**
b. Explain 4 bit shift register (non inverting) using NMOS logic. **(10 Marks)**

6 a. Design a 4 bit adder to implement addition, subtraction, XOR, XNOR, OR and AND operations. **(08 Marks)**
b. Draw the basic form of a 2 phase clock generator and explain. **(06 Marks)**
c. What are the system timing considerations in system design? **(06 Marks)**

7 a. Explain 3 transistor dynamic RAM cell. **(06 Marks)**
b. Explain Braun array multiplier with a neat diagram. **(06 Marks)**
c. What are the ground rules required for successful design? **(08 Marks)**

8 Write short notes on:
a. Transmission gate.
b. BiCMOS logic.
c. Input output pads.
d. BIST. **(20 Marks)**

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